



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Kenji YOSHIDA, et al.

SERIAL NO: 10/642,222

GAU: 2812

FILED: August 18, 2003

EXAMINER:

FOR: METHOD OF ACCELERATING TEST OF SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

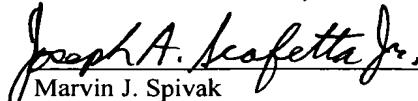
- Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 241677US2	SERIAL NO. 10/642,222		
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Kenji YOSHIDA, et al.					
		FILING DATE August 18, 2003		GROUP 2812			
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	5,930,587	07/27/1999	V. W. RYAN			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AO						
	AP						
	AQ						
	AR						
	AS						
	AT						
	AU						
	AV						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	K. YOSHIDA, et al., International Electron Device Meeting, pages 753-756, "STRESS-INDUCED VOIDING PHENOMENA FOR AN AACTURAL CMOS LSI INTERCONNECTS", December 2002					
	AX						
	AY						
	AZ					<input type="checkbox"/> Additional References sheet(s) attached	
Examiner				Date Considered			
<p>*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							



LIST OF RELATED CASES

<u>Docket Number</u>	<u>Serial or Patent Number</u>	<u>Filing or Issue Date</u>	<u>Inventor/Applicant</u>
232464US2S	10/337,402	01/07/03	MIYAMOTO et al.
241677US2*	10/642,222	08/18/03	YOSHIDA et al.

*Present Application; listed for information

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